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EXAMINER	
OSBORNE, LUKE R	
ART UNIT	**PAPER NUMBER**
2123	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/076,920	DELIWALA, SHRENIK	
	Examiner	Art Unit	
	Luke Osborne	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 September 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *44,47,48,55,56 and 58* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *44,47,48,55,56 and 58* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 September 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Status

1. Claims 44, 47, 48, 55, 56, and 58 are pending in the instant application.

Claims 44, 47, 48, 55, 56, and 58 stand rejected.

Response to Arguments

2. Applicant's arguments with respect to claims 44, 47, 48, 55, 56, and 58 have been considered but are moot in view of the new ground(s) of rejection.

Applicant's arguments with respect to claims 50 and 51have been considered but are moot since those claims are cancelled along with claim 49.

Drawings

3. The drawings were received on 9/24/2007. These drawings are acceptable.

Claim Objections

4. Claim 44 contains the acronym "SOI" used as "SOI-based". In order to reduce possible confusion all acronyms should be expanded upon first use. Appropriate correction is required.

Specification

5. The substitute specification received on 9/24/2007 is acceptable.

Claim Rejections - 35 USC § 112

6. Examiner acknowledges the amendment to claim 55. Consequently the rejection is withdrawn.

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claims 44, 47, 48, 55, 56, and 58 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 44, line 14 contains the limitation of "co-simulating". It is unknown what Applicant's intending to claim as no support for that term is found in the application as filled.

In the interest of a compact prosecution the broadest reasonable interpretation has been applied in the absence of a particular definition. The Examiner interprets the "co" part of the "co-simulating" to imply that the simulation of the SOI-based integrated optical/electronic circuit requires two different simulations the output of the electrical based simulation coupled to the optical analysis.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 44, 55, 56, 58 are rejected under 35 U.S.C. 102(b) as being anticipated by an article "Improving the Response of Optical Phase Modulators in SOI by computer Simulation" by P. D. Hewitt et al., hereinafter "Hewitt".

Regarding claim 44, Hewitt discloses a method of operating a computer processor, the computer processor using computer software, the computer software being configured to simulate both the electrical characteristics and the optical characteristics of an SOI-integrated optical/electronic circuit, the method comprising:

simulating operation of a least certain electronic circuit components of said SOI-based integrated optical/electronic circuit using an electronic design portion of the computer software [Hewitt: The two-dimensional simulation package SILVACO (Page 444, Section IV Electrical and Optical Analysis)] to generate as outputs dopant profiles [Hewitt: Figure 7, page 447 right column], topology information [Hewitt: page 446, section B. Device characteristics for the modulator with rounded edges] and free-carrier concentration information and time-dependent variation in the free-carrier concentration as a function of applied voltage [Hewitt: injected free carrier densities in the intrinsic

region of the device for a range of different device geometries and working conditions (Page 445, left column, first paragraph)];

applying the output information from the electronic design portion of the computer software as inputs to an optical design portion of the computer software [A 2-D semiconductor simulation package SILVACO was employed to investigate the dc and transient behavior of the active region of the modulator, via the solution of the Poisson and continuity equations. It was demonstrated that a high degree of uniformity of the injected carrier concentrations is predicted in the guided region of the modulator, thus simplifying the optical mode analyses (Page 449, right column, section VI, 2nd paragraph)] to extract top-level optical parameters such as optical loss [Hewitt: Losses as low as 0.3 dB/cm have been demonstrated for SOI waveguides (Page 443, right column first paragraph)], optical phase [Hewitt: The change in refractive index results in a phase shift in the optical mode given by (page 445, left column, first full paragraph)] and extinction (loss as disclosed above); and

co-simulating electrical and optical behavior of said integrated optical/electronic circuit through said electrical and optical computational engines to predict the optical behavior of said SOI-based integrated optical/electronic circuit [From at least the broadest reasonable interpretation as given above as being a electrical then optical analysis of the circuit. These limitations are found in Section IV Electrical and Optical Analysis, starting on page 444].

Regarding claim 55 Hewitt discloses the method of claim 44, wherein the optical design portion of the computer software partially models a waveguide included in said at least certain optical circuit components of the SOI-based integrated optical/electronic circuit [Hewitt: The device structure to be considered in this paper is of a lateral optical phase modulator integrated into a low loss SOI rib waveguide (Page 444, Section III Device Structure, first paragraph)].

Regarding claim 56 Hewitt discloses the method of claim 55, wherein the SOI circuit includes a substrate later, and wherein the waveguide at least partially extends within said substrate layer [Hewitt: Figure 1, page 444].

Regarding claim 58 Hewitt discloses the method of claim 44, wherein the electronic design portion of the computer software simulates at least one electronic circuit component from the group of a p-n device, a field plated device, an avalanche photodiode, a Schottky device, a MOSCAP, and a MOSFET [Hewitt: The effects on the device performance due to changes in doping concentrations, doping diffusion depths and doping profiles of the p and n regions has been investigated.(Page 447, Section C, first paragraph)].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 47 and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hewitt in view of Applicant's Admitted Prior Art (AAPA).

Regarding claim 47 Hewitt teaches the method of claim 44, wherein the electronic design portion of the computer software as addressed above.

Hewitt does not expressly teach that the electronic design portion includes at least one of the group consisting of a process simulation portion, a device simulation portion, a layout portion, a parasitic extraction portion, and a circuit simulation portion.

AAPA teaches from paragraph [0437] on page 127 from the clean specification submitted on 9/24/2007 that

AAPA: In the embodiment shown in FIG. 89, the EDA portion 8202 includes a layout portion 8206, a process simulation portion 8208, a device simulation portion 8210, a circuit simulation portion 8212, and a parasitic extraction portion 8214. These electronic portions are intended to be illustrative in nature, but not limiting in scope. **The specific tools that are included in the EDA portion 8202 are a design choice. Any suitable one or more computer program or electronic simulation engine may be included in the EDA portion 8202, and remain within the scope of the present invention.** (emphasis added)

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use Applicant's admission that software existed to perform the functions called out in the claimed limitations in order to enhance any software as a matter of design choice. Such a choice was available to Hewitt.

The motivation to do so would have been as Applicant's clearly identify in the admission that adding these features are a matter of design choice.

Regarding claim 48 Hewitt teaches the method of claim 44, wherein said optical design portion of the computer software produces an optical analysis as taught above.

Hewitt does not expressly teach that the analysis comprises at least one of the croup consisting of: a finite difference time domain (FDTD) portion, a beam propagation method portion, and a raytracing portion.

AAPA from paragraph [0437] on page 127-128 from the clean specification submitted on 9/24/2007 that

Similarly, the embodiment of optical simulation design tool portion 8204 includes a gratings/DOE portion 8222, a finite different time domain (FDTD) portion 8220, a thin film portion 8224, a raytracing portion 8226, and a beam propagation method portion 8228. These optical portions are intended to be illustrative in nature, but not limiting in scope. **The specific tools that are included in the optical simulation design tool portion 8204 are a design choice. Any suitable one or more computer program or electronic simulation engine may be included in the optical simulation design tool portion 8204, and remain within the scope of the present invention.**

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use Applicant's admission that software existed to perform the functions called out in the claimed limitations in order to enhance any software as a matter of design choice. Such a choice was available to Hewitt.

The motivation to do so would have been as Applicant's clearly identify in the admission that adding these features are a matter of design choice.

10. Claims 44, 47, 48, 55, 56, and 58 rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA.

Regarding claim 44, AAPA teaches a method of operating a computer processor, the computer processor using computer software, the computer software being configured to simulate both the electrical characteristics and the optical characteristics of an SOI-integrated optical/electronic circuit, the method comprising:

simulating operation of a least certain electronic circuit components of said SOI-based integrated optical/electronic circuit using an electronic design portion of the computer software to generate as outputs dopant profiles, topology information and free-carrier concentration information and time-dependent variation in the free-carrier concentration as a function of applied voltage;

applying the output information from the electronic design portion of the computer software as inputs to an optical design portion of the computer software to extract top-level optical parameters such as optical loss, optical phase and extinction; and

co-simulating electrical and optical behavior of said integrated optical/electronic circuit through said electrical and optical computational engines to predict the optical behavior of said SOI-based integrated optical/electronic circuit.

Applicants state from paragraph [0400] that

> For example, detailed topology, dopant profile and index profile can be generated for passive SOI waveguide structures and thus can be fed into the optical simulation design tool portion 8204 to be used to model optical passives. In order to model active opto-electronic devices, a device physics simulator is also used to compute free carrier concentration in Si as a function of voltage applied to vacuum electrodes. This time dependent and space dependent concentration (and therefore the ability to derive effective mode index) is fed into, for example, PDTD to produce spatial and temporal behavior of optical beams. This optical behavior can then be used to extract "top-level" optical parameters such as phase, extraction, chirp, extinction, and/or other such parameters. **It is emphasized that there are a wide variety of electronics engines and optical engines that may be utilized in the EDA portion 8202 and optical simulation portions.**

Applicant's state previously in paragraphs 436 and 437 that well known EDA tools are used to perform these functions and that the use of any particular EDA tool would be design choice.

Therefore any specific combination of features as recited by claim 44 as Applicant's state in pages 127-128 are a matter of the combination of admitted technologies that existed at the time of the invention and design choice.

The Examiner notes that the combination of prior art technologies for their intended purposes could be patentable with the evaluation of secondary considerations, in the instant application Applicant's clearly teach that any particular implementation of the technologies as claimed are a matter of design choice.

Similarly the limitations recited in claims 47, 48, 55, 56 and 58 are taught by AAPA from paragraphs 436-440 from pages 127-128.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luke Osborne whose telephone number is (571) 272-4027. The examiner can normally be reached on 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul L. Rodriguez can be reached on (571) 272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

LRO

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